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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,448	11/25/2003	Astrid Elbe	S0193.0010	5966
38881	7590	08/09/2006		EXAMINER
DICKSTEIN SHAPIRO LLP 1177 AVENUE OF THE AMERICAS 6TH AVENUE NEW YORK, NY 10036-2714			PAN, DANIEL H	
			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 08/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/723,448	ELBE ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 25 November 2003.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-14 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-14 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 25 November 2003 is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1.) Certified copies of the priority documents have been received.  
 2.) Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3.) Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | Paper No(s)/Mail Date: _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>07/22/05.02/02/04</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____                                    |

Claims 1-14 are presented for examination.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 2,4-8 are rejected under 35 U.S.C. 102(b) as being anticipated by

O'Connor et al. (6,026,485).

2. As to claim 1, O'Connor taught a processor as claimed including at least :

a) an arithmetic unit for processing operands (see integer and floating point units in fig.1 );

b) a register memory for storing operands (see fig.8, see also fig.4 B for background of the memory space); and

c) a register memory configuration unit (see fig.4C stack management unit ) designed to configure the register memory such that memory space in the register memory is assigned to operands (see operand memory stack region in fig.8) and that memory space in the register memory that is not assigned to operands is made available for

other data than the operand (see constant pool or local variables space in fig.8, see also fig.11 for the operand to the execution unit);

- d) peripheral devices (see I/O bus in fig.1);
- e) host cpu (see the CPU IN col.7, lines 28-34)

3. As to claim 2, O'Connor also included a single chip (see Internet chip in col.8, lines 8-15).

4. As to claim 4, O'Connor also included external memory (see external memory in fig.1).

5. As to claim 5, O'Connor also included algorithm (see size defined in the program long in col.41, lines 35-40) for maximum length and algorithm (see size defined short in col.41, lines 35-40 ) smaller length .

6. As to claim 6, see the encryption in col.2, lines 49-57.

7. As to claim 7, also included internal bus (see internal bus in fig.1).

8. As to claim 8, O'Connor also configured the register memory in different length as needed (see the single word entry and double word entries I col.42, lines 36-67, col.43, lines 1-1-2).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over O'Connor et al. (6,026,485) Hadad (6,185,596).

As to claim 3, O'Connor did not specifically show his operand was more than 150 bits as claimed. However, Hadad taught in a system that there is no theoretical length limit of the expend (see col.3, lines 20-30). Therefore, it would have been obvious to one of ordinary skill in the art to use Hadad in O'Connor for including the 150 bit operand as claimed because the use of Hadad could provide O'Connor the ability to adapt to s different operand width, and therefore, increasing the flexibility of O'Connor's operand processing , and Because O'Connor also disclosed that the number and size of operands was determined by the opcode (see col.44, lines 61-67), which was a suggestion of the need for including longer operand words in order to adapt to the increasing complexity for the arithmetic instructions , such as the longer length of instruction opcode, for the above reasons, provided a motivation.

10. Claims 9-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Boettner et al. (4,777,589).

11. As to claims 9, 11, Boettner taught a computer system as claimed including at least :

a) a host CPU (see system processor in fig.1);

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b) a peripheral device connected to the host CPU via an external bus comprising an internal memory (see peripheral or I/O in fig.1) and  
c) a memory configuration unit, the memory configuration unit being designed to make space from the internal memory available for the peripheral device as needed (see memory mapped I/O in col.1, lines 19-37, the privileged memory page in col.2, lines 8-41), and to make space from the internal memory not being made available to the peripheral device available for (see unprivileged page in col.2, lines 8-41).

As to claim 10, Boettner also included an internal memory like external memory (see unprivileged memory page).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Boettner et al. (4,777,589) in view of Cunningham et al. (5,659,680)

As to claim 12, limitations of parent claim already discussed in previous paragraph.

Boettner did not specifically teach making the internal memory into working memory when the peripheral device was not active as claimed. However, Cunningham disclosed a system for opening a hidden internal memory area or protected memory

I/O (see col.24, lines 45-62 ). It would have been obvious to one of ordinary skill in the art to use Cunningham in Boettner for making internal memory into working memory (e.g. open) when the peripheral is not active as claimed because the use of Cunningham could provide Boettner the control capability to adapt to particular system memory condition (e.g. the available memory space) as needed, and Boettner also disclosed mapping of the virtual memory address space to the physical memory (see col.1, lines 13-18) , which was a suggestion of need for making additional memory space available for use, such as a working memory, or the like, and for doing so, provided a motivation.

13. Claims 13,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boettner et al. (4,777,589) in view of O'Connor et al. (6,026,485).

14. As to claims 13,14, limitations of parent claim already discussed in previous paragraph. Boettner did not specifically show the cryptographic processor as claimed. However, O'Connor disclosed cryptographic system ( see the encryption in col.2, lines 49-57). It would have been obvious to one of ordinary skill in the art to use O'Connor in Boettner for including the cryptographic processor as claimed because the use of O'Connor could expand the processing capability of Boettner to accept processing specific system security, such as the encryption taught by O'Connor, and because Boettner did show concern for system protection, which provided a suggestion for crypto processing , or the like (see col.6, lines 31-36).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

## **21 Century Strategic Plan**

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PRIMARY EXAMINER  
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